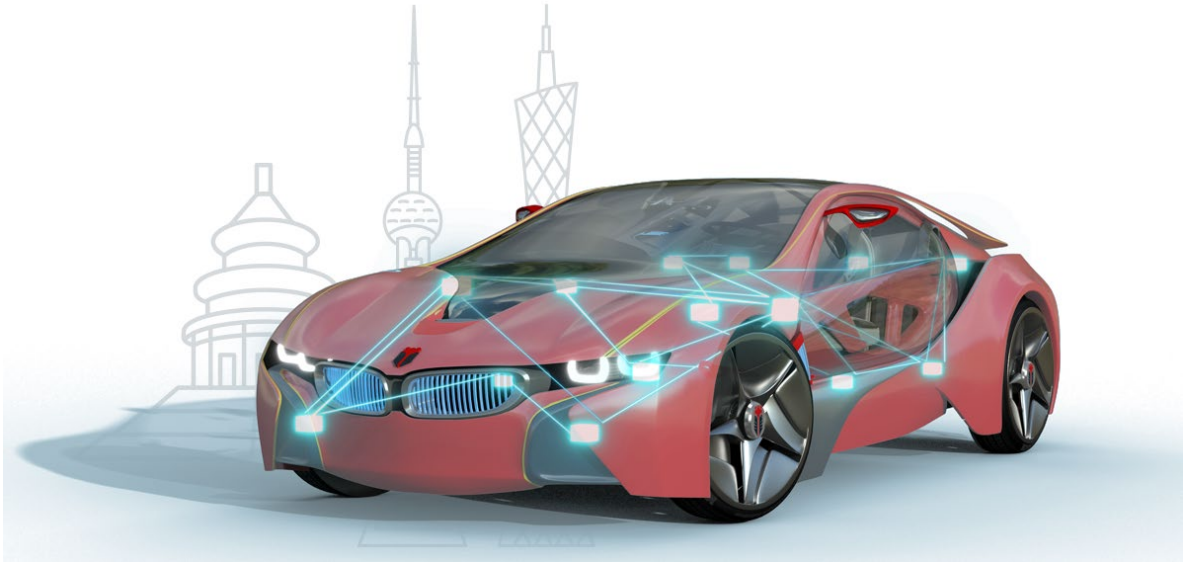
英飞凌 TC3XX_Cache 和 Overlay 功能详解

DETAILED EXPLANATION OF INFINEON TC3XX_CACHE AND OVERLAY FUNCTIONS



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DETAILED EXPLANATION OF INFINEON TC3XX_CACHE AND OVERLAY FUNCTION

1 概述 OVERVIEW

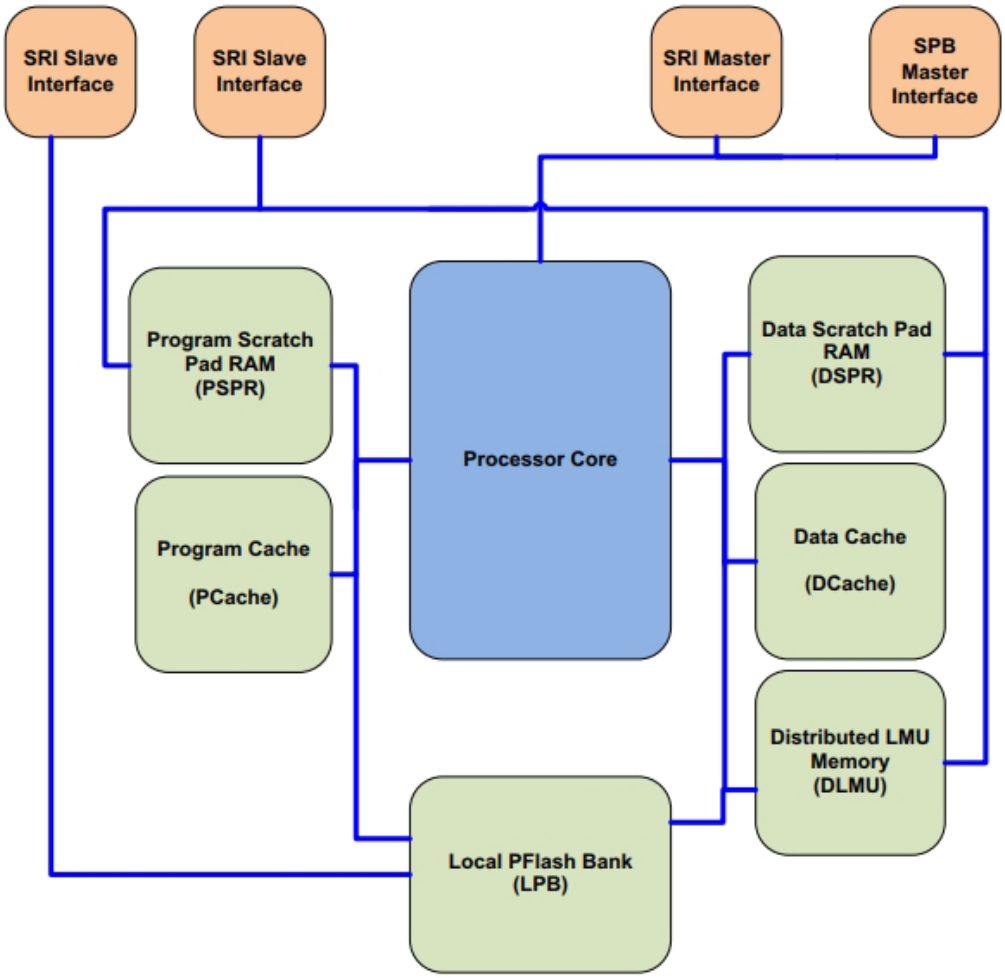
英飞凌 AURIX™ TC3XX 系列微控制器是面向汽车电子和工业控制领域的高性能多核处理器平台，其架构设计充分考虑了实时性、功能安全（ISO 26262）和信息安全的需求。该系列采用 TriCore™异构多核架构，结合了精简指令集计算机（RISC）和复杂指令集计算机（CISC）的特征，整合了 32 位 RISC CPU、DSP 运算单元和专用外设控制器，主频可达 300MHz，内置 HSM（硬件安全模块），在 ASIL-D 级功能安全认证和信息安全防护方面具有显著优势。在存储子系统设计上，TC3XX 创新性地融合了缓存（Cache）机制和数据访问覆盖（Data Access Overlay）技术，有效解决了汽车电子系统中实时数据处理与存储访问效率的关键矛盾。

The Infineon AURIX™ TC3XX family of microcontrollers is a high-performance, multi-core processor platform for automotive electronics and industrial control, with an architecture designed with real-time, functional safety (ISO 26262) and information security in mind. The TriCore™ heterogeneous multi-core architecture combines the features of a RISC (Reduced Instruction Set Computer) and a CISC (Complex Instruction Set Computer), integrating a 32-bit RISC CPU, a DSP unit and dedicated peripheral controllers, with a main frequency of up to 300MHz, and a built-in HSM (Hardware Security Module), which provides significant advantages in terms of ASIL-D functional safety certification and information security protection. The built-in HSM (Hardware Security Module) provides significant advantages in ASIL-D level functional safety certification and information security protection. In terms of storage subsystem design, TC3XX innovatively integrates the Cache mechanism and Data Access Overlay technology, effectively solving the key contradiction between real-time data processing and storage access efficiency in automotive electronic systems.

2 CACHE 模块概述 CACHE OVERVIEW

TC3XX 的缓存系统分为 PCache(指令缓存)和 DCache(数据缓存)，Cache 内部组成包含 Cache 控制器和两块 SRAM (Tag RAM、DATA RAM)。程序缓存(PCACHE)采用两路组相联的缓存结构，每组有两个缓存行可选，每个缓存行大小为 256 位。针对汽车电子典型的总线访问模式，缓存控制器使用了最近最少使用算法（LRU）进行缓存替换。因此当缓存满时，替换最长时间未使用的缓存行。在 ADAS 传感器数据处理场景中可实现较高缓存命中率。

The cache system of TC3XX is divided into PCache (Instruction Cache) and DCache (Data Cache), and the internal composition of Cache includes Cache controller and two SRAMs (Tag RAM, DATA RAM). The Program Cache (PCACHE) adopts a two-way group-connected cache structure, with two cache lines available in each group, and the size of each cache line is 256 bits. For the typical bus access pattern of automotive electronics, the cache controller uses the Least Recently Used (LRU) algorithm for cache replacement. Thus, when the cache is full, the longest unused cache line is replaced. A high cache hit rate can be achieved in ADAS sensor data processing scenarios.



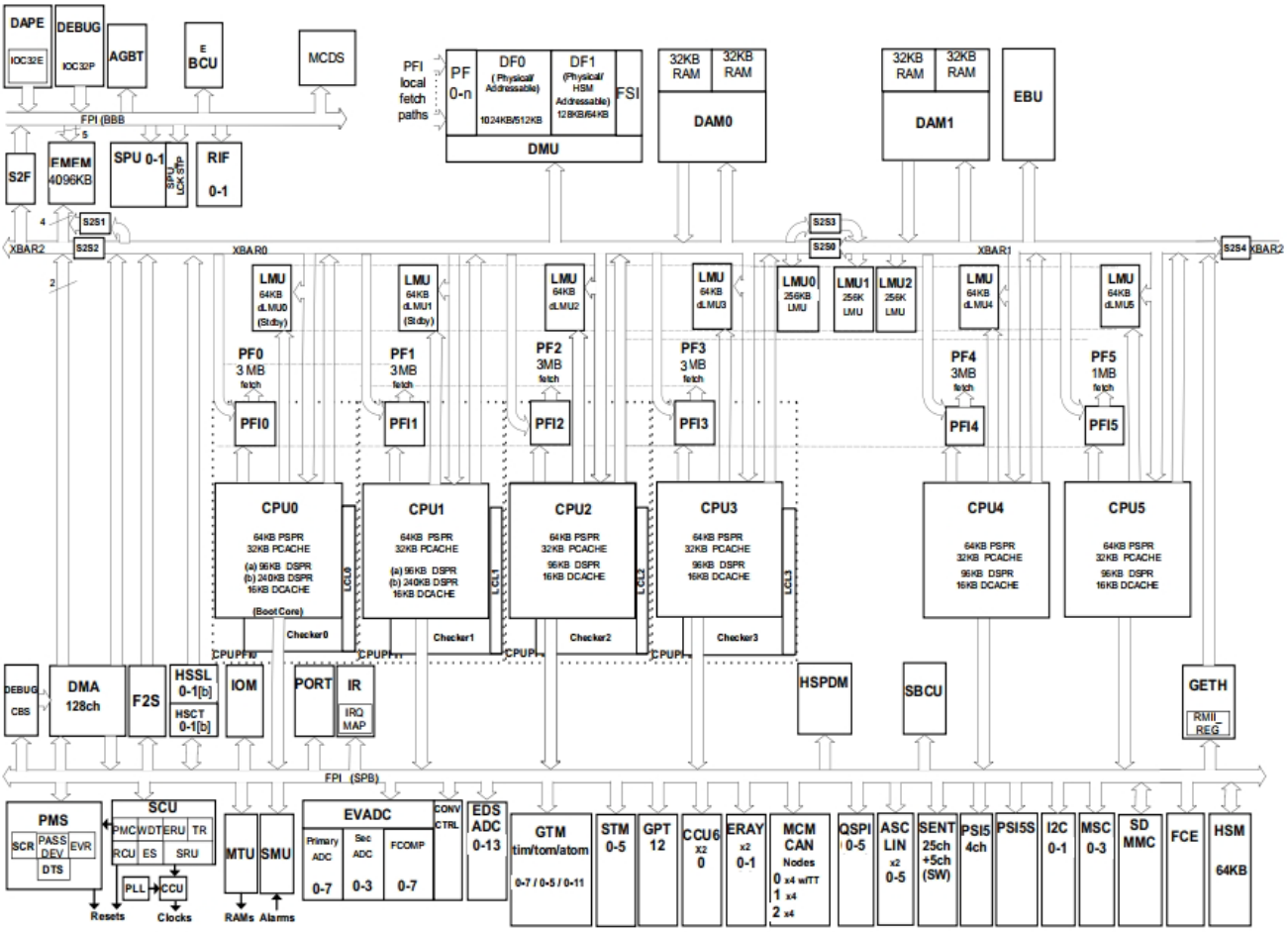
3 内存空间概述 MEMORY SPACE OVERVIEW

TC3XX 采用先进的 32 位架构，实现了一个全面而复杂的内存系统。其内存空间的设计充分考虑了现代汽车电子系统对高性能、实时性和功能安全的严格要求。整个内存系统采用分层设计理念，包括非易失性存储器（程序闪存和数据闪存）、多级 RAM 系统（本地 SRAM、全局 SRAM 和局部存储单元 LMU）以及 A/B 分区。这种多层次的存储架构不仅确保了数据访问的高效性，还通过多重保护机制维护了系统的安全性和可靠性。

TC3XX employs an advanced 32-bit architecture, implementing a comprehensive and sophisticated memory system. Its memory space design fully considers the strict requirements of modern automotive electronic systems for high performance, real-time capability, and functional safety. The entire memory system adopts a layered design philosophy, including non-volatile memory (program flash and data flash), multi-level RAM system (local SRAM, global SRAM, and Local Memory Unit LMU), as well as A/B banks. This multi-tiered storage architecture not only ensures efficient data access but also maintains system security and reliability through multiple protection mechanisms.

此外，所有总线主设备都可以在相同地址访问相同的外设和存储器。系统地址映射对所有 CPU 都是可见且有效的，这意味着所有外设和资源都可以被所有 TriCore CPU 和其他片上总线主设备访问。当然，也可以借助总线 MPU(存储器保护单元)根据需求，配置不同细粒度的访问控制来保护关键的存储器区域。具体来说，MPU 包含了三个主要的保护组件：首先是八个读写保护的暂存器存储器区域(PSPR、DSPR)，可以针对每个总线主设备独立配置其读写权限；其次是八个读写保护的 DLMU(本地存储器单元)区域，同样支持基于主设备的权限控制；最后是针对本地 PFlash 存储体(LPB)访问的独立主设备读取使能。这种多层次、细粒度的内存系统机制不仅提供了足够的灵活性来满足不同应用场景的需求，还确保了系统的数据访问安全性。

Furthermore, all bus master agents can access identical peripherals and memories at identical addresses. The system address map is visible and valid for all CPUs, meaning that all peripherals and resources are accessible by all TriCore CPUs and other on-chip bus master agents. Of course, the bus MPU (Memory Protection Unit) can be utilized to configure access controls of different granularity to protect critical memory regions as needed. Specifically, the MPU contains three main protection components: first, eight read-write protected scratch pad memory regions (PSPR, DSPR), which can be independently configured for read-write permissions for each bus master; second, eight read-write protected DLMU (Local Memory Unit) regions, which similarly support master-based permission control; and finally, independent master read enables for accessing the local PFlash Bank (LPB). This multi-level, fine-grained memory system mechanism not only provides sufficient flexibility to meet the requirements of different application scenarios but also ensures the security of system data access.


DAPE
DEBUG
AGBT
BCU
MCDS
PFI local fetch paths
PF 0-n
DF0
DF1
FSI
DMU
32KB RAM
DAM0
DAM1
EBU
FPI (BBB)
S2F
FMEM 4096KB
SPU 0-1
RIF 0-1
XBAR2
XBAR0
XBAR1
S254
LMU
LMU0
LMU1
LMU2
PF0 3 MB
PF1 3MB
PF2 3MB
PF3 3MB
PF4 3MB
PF5 1MB
PFI0
PFI1
PFI2
PFI3
PFI4
PFI5
CPU0
CPU1
CPU2
CPU3
CPU4
CPU5
Checker0
Checker1
Checker2
Checker3
DEBUG CBS
DMA 128ch
F2S
HSSL 0-1[b]
HSCT 0-1[b]
IOM
PORT
IR
IRQ MAP
HSPDM
SBCU
GETH
RMII REG
FPI (SPB)
PMS
SCR
PASS
DEV
EVR
DTS
SCU
PMC
WDT
ERU
TR
RCU
ES
SRU
PLL
CCU
Resets
Clocks
MTU
SMU
RAMs
Alarms
EVADC
Primary ADC
Sec ADC
FCOMP
CONV CTRL
EDS ADC 0-13
GTM tim/tom/atom
STM 0-5
GPT 12
CCU6 x2 0
ERAY x2 0-1
MCM CAN Nodes
QSPI 0-5
ASC LIN x2 0-5
SENT 25ch +5ch (SW)
PSI5 4ch
PSI5S
I2C 0-1
MSC 0-3
SD MMC
FCE
HSM 64KB

4 地址访问重映射机制 DATA ACCESS OVERLAY OVERVIEW(OVC)

TriCore 内核中的 Overlay 功能是一种高效的数据访问重定向机制，它允许将程序 Flash、在线数据采集空间或 EBU (External Bus Unit) 空间的特定数据访问重定向到覆盖存储器中。这些覆盖存储器可以灵活地配置在多个位置，包括本地存储器、仿真存储器、EBU 空间或 DPSR/PSPR 存储器。这种机制的一个重要特点是它只重定向读写数据访问，而不会影响其他操作，并且在执行重定向时不会带来任何性能损失。这种设计特别适用于需要在程序运行时动态修改 Flash 中存储的测试和标定参数的场景，为实时系统的参数调整和数据采集提供了灵活且高效的解决方案。通过这种方式，开发人员可以在不中断系统运行的情况下，实现对关键参数的实时修改和监控，这在汽车电子等要求严格的嵌入式系统中具有重要的应用价值。

Data access overlay is an efficient data access redirection mechanism that allows specific data accesses from the TriCore processor to Program Flash, Online Data Acquisition space, or EBU (External Bus Unit) space to be redirected to overlay memory. These overlay memories can be flexibly configured in multiple locations, including Local Memory, Emulation Memory, EBU space, or DPSR/PSPR memory. A key feature of this mechanism is that it only redirects read and write data accesses without affecting other operations, and performs the redirection without any performance penalty. This design is particularly suitable for scenarios where test and calibration parameters stored in Flash need to be modified dynamically during program runtime, providing a flexible and efficient solution for parameter adjustment and data acquisition in real-time systems. Through this approach, developers can achieve real-time modification and monitoring of critical parameters without interrupting system operation, which has significant application value in embedded systems with strict requirements, such as automotive electronics.

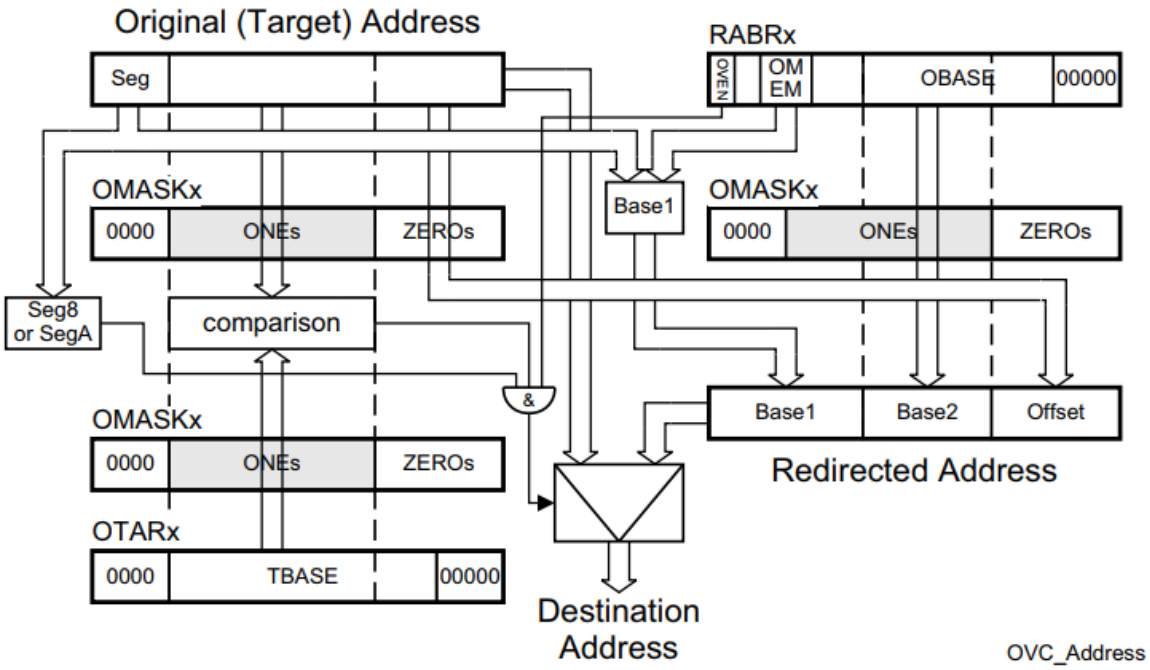
TC397xx 的 Overlay 系统是一个功能强大且灵活的数据访问重定向机制，它能够将对程序 Flash、OLDA 或外部 EBU 空间的数据访问重定向到不同位置的覆盖存储器中，包括本地存储器(LMU)、仿真存储器、EBU 空间以及 DSPR 或 PSPR 存储器。系统支持高达 4MB 的覆盖存储器地址范围，每个 TriCore 内核最多可配置 32 个 Overlay 块，单个 Overlay 块大小可从 32 字节到 128KB 不等。每个区块都可以独立配置其存储器位置和大小，并且支持通过单次寄存器写入操作同时控制多个区块的启用或禁用。系统还提供了数据缓存的可编程刷新控制，确保覆盖操作与数据加载同步进行。特别值得注意的是，每个处理器核心都配备了独立的 Overlay 系统，这种设计极大地提高了系统的灵活性和可用性，使其能够满足各种复杂应用场景的需求。

The Overlay function in TC397xx is a powerful and flexible data access redirection mechanism that can redirect data accesses from Program Flash, OLDA, or external EBU space to overlay memory in different locations, including Local Memory (LMU), Emulation Memory, EBU space, and DSPR or PSPR memory. The system supports an overlay memory address range of up to 4MB, with each TriCore core capable of configuring up to 32 Overlay blocks, ranging in size from

32B to 128KB per block. Each block can be independently configured for its memory location and size, and multiple blocks can be enabled or disabled through a single register write operation. The system also provides programmable refresh control for data cache, ensuring synchronization between overlay operations and data loading. Notably, each processor core is equipped with its own independent Overlay system, a design that greatly enhances the system's flexibility and usability, enabling it to meet the requirements of various complex application scenarios.

如下图所示，对 0x8H 段或 0xAH 段的任何数据访问都会与所有激活的 Overlay 块进行检查匹配。对于每个激活的区域，系统会将地址位与目标基地址(OTARx)进行比较，这个按位比较由 OMASKx 寄存器的内容来限定。只有当对应的 OMASKx 位被设置为 1 时，相应的地址位才会参与比较。当所有由 OMASKx 选择的地址位与 OTARx 寄存器中的对应位相等时，才会触发访问重定向。这种机制确保了精确的地址匹配和灵活的覆盖范围控制。

As shown in the following figure, any data access to segment 0x8H or 0xAH is checked against all activated Overlay blocks. For each activated area, the system compares the address bits with the target base address (OTARx), and this bit-wise comparison is qualified by the content of the OMASKx register. Address bits only participate in the comparison when the corresponding OMASKx bits are set to 1. Access redirection is triggered only when all address bits selected by OMASKx match the corresponding bits in the OTARx register. This mechanism ensures precise address matching and flexible control of overlay ranges.



在 TC3xx 芯片中，Cache 和 Overlay 的配合使用需要综合考虑性能和可靠性。首先，对于程序缓存(PCACHE)建议保持开启以提高指令访问效率，而数据缓存(DCACHE)则需要根据 Overlay 的具体使用场景来灵活配置。对于频繁访问但较少更新的 Overlay 区域，建议开启缓存以提高访问速度；对于需要实时更新的数据区域，可以考虑使用缓存旁路模式以确保数据的实时性。在数据布局方面，应当将频繁访问的数据放在同一 Overlay 块中，并使块大小尽可

能对齐到 Cache line，以提高缓存效率。对于多核场景，每个核心都应该有其独立的 Overlay 配置，避免相互干扰的同时也保证了各个核数据访问时重定向功能的有效性。同时，在进行 Overlay 数据更新时，需要注意使用 DMI 提供的缓存刷新控制，确保 Cache 和内存数据的一致性。此外，还应建立必要的错误处理机制，以应对可能出现的 Cache 同步或 Overlay 访问错误。通过这些优化措施，可以充分发挥 Cache 和 Overlay 的性能优势，同时保证系统的可靠性。

In TC3xx chips, the combined use of Cache and Overlay requires comprehensive consideration of both performance and reliability. First, it is recommended to keep the program cache (PCACHE) enabled to improve instruction access efficiency, while the data cache (DCACHE) needs to be flexibly configured according to specific Overlay usage scenarios. For Overlay areas that are frequently accessed but rarely updated, enabling cache is recommended to improve access speed; for data areas requiring real-time updates, cache bypass mode can be considered to ensure data timeliness. Regarding data layout, frequently accessed data should be placed in the same Overlay block, and block sizes should be aligned with Cache lines whenever possible to improve cache efficiency. In multi-core scenarios, each core should have its independent Overlay configuration, not only preventing mutual interference but also ensuring the effectiveness of redirection functionality during data access by each core. Meanwhile, when updating Overlay data, attention must be paid to using the cache refresh control provided by DMI to ensure consistency between Cache and memory data. Additionally, necessary error handling mechanisms should be established to address potential Cache synchronization or Overlay access errors. Through these optimization measures, the performance advantages of both Cache and Overlay can be fully utilized while ensuring system reliability.

5 OVERLAY 功能应用示例 EXAMPLE OF DATA ACCESS OVERLAY

5.1 使能各核的 Overlay 块区。Enable Overlay Block for each core.

CPUx Overlay Range Select Register

OSEL
CPUx Overlay Range Select Register (0FB00$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SHOVEN_x															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHOVEN_x															
rw															

Field	Bits	Type	Description
SHOVEN_x	31:0	rw	**Shadow Overlay Enable - SHOVEN[x]** One enable bit is provided for each of the 32 overlay blocks. 00000000_H Overlay block x is disabled when OVCCON.OVSTRT is set. 00000001_H Overlay block x is enabled when OVCCON.OVSTRT is set.

OVCENABLE
Overlay Enable Register (01E0$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										OVEN5	OVEN4	OVEN3	OVEN2	OVEN1	OVEN0
r										rw	rw	rw	rw	rw	rw

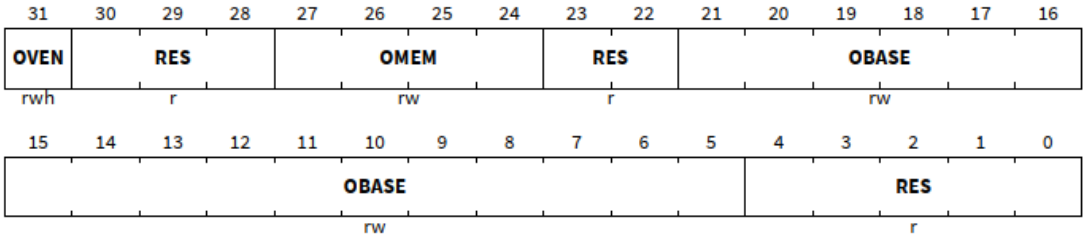
Overlay 块区选择寄存器和 Overlay 功能使能寄存器，每个 core 都有 32 个可配置的 overlay block，每个 block 的使能和关闭都对应着寄存器的一个 bit。

Overlay Range Select Register for each overlay block and Overlay Enable Register for all cores. Each core has 32 configurable overlay blocks, and the enable and disable of each block corresponds to one bit in the range select register.

5.2 选取重映射地址：即 CPU 最终会访问的 RAM 地址。Select the redirected address: The RAM address that the CPU will eventually access.

CPUx Redirected Address Base Register i

RABRi (i=0-31)
CPUx Redirected Address Base Register i **($0FB10_H$+i*12)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RES	4:0, 23:22, 30:28	r	**Reserved** Reads as 0; should be written with 0.
OBASE	21:5	rw	**Overlay Block Base Address** Bits 21..5 of the base address the overlay memory block in the overlay memory. If the corresponding bit in OMASK register is set to one, OBASE bit value is used in the redirection address. If the corresponding bit in OMASK register is set to zero, OBASE bit value is ignored.

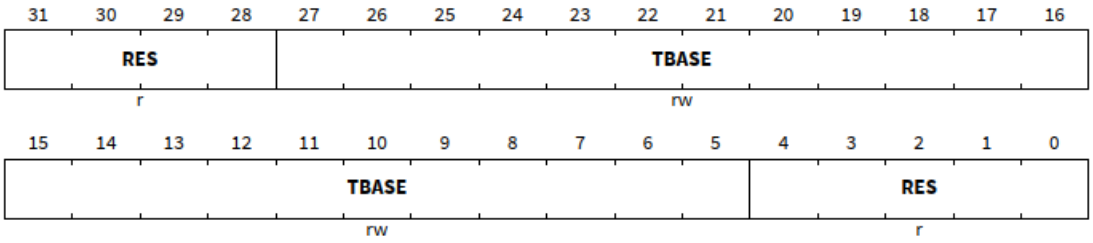
Field	Bits	Type	Description
OMEM	27:24	rw	**Overlay Memory Select** Selects overlay memory used for redirection. 0_H Redirection to Core 0 DSPR/PSPR memory 1_H Redirection to Core 1 DSPR/PSPR memory 2_H Redirection to Core 2 DSPR/PSPR memory 3_H Redirection to Core 3 DSPR/PSPR memory 4_H Redirection to Core 4 DSPR/PSPR memory 5_H Redirection to Core 5 DSPR/PSPR memory 6_H Reserved 7_H Reserved 8_H Redirection to LMU 9_H Redirection to EMEM A_H Redirection to EBU B_H Reserved … F_H Reserved
OVEN	31	rwh	**Overlay Enabled** This bit controls whether the overlay function of overlay block x is enabled. This bit can also be changed when OVCCON.OVSTP or OVCCON.OVSTRT is set. See OVCCON register description. 0_B Overlay function of block x is disabled. 1_B Overlay function of block x is enabled.

重映射地址基础配置寄存器， OBASE 字段用于配置标定区域的基地址。需要在 OMEM 类型/区域选择的基础上，从其基地址开始偏移的，LMU、DSPR 等 RAM 区域均支持配置。

Redirected Address Base Register, OBASE field is used to configure the base address of the calibrated region. It needs to be offset from its base address based on the OMEM type/region selection, and the configuration is supported for RAM regions such as LMU and DSPR.

5.3 选取目标地址：即 CPU 访问的数据的 DFLASH 地址。Select the target address: the DFLASH address of the data accessed by the CPU.

OTARi (i=0-31)
CPUx Overlay Target Address Register i **($0FB14_H$+i*12)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RES	4:0, 31:28	r	**Reserved** Reads as 0; should be written with 0.

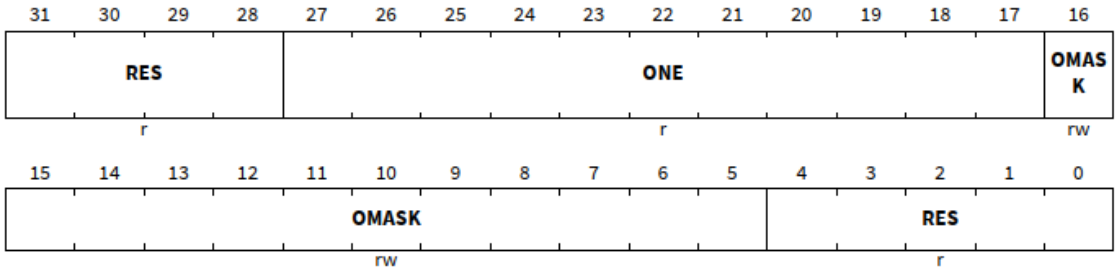
重定向目标地址配置寄存器，主要配置的就是需要重映射的地址，0x8h 或 0xAh 开头范围内的 Flash 区域，如 PFlash、DFlash 和前边提到的外部总线单元地址 EBU 均可选取配置。

Overlay Target Address Register, the main configuration is the need to remap the address, 0x8h or 0xAh beginning range of the Flash region, such as PFlash, DFlash and the previously mentioned external bus unit address, EBU can be selected to configure here.

5.4 选取 Overlay 块区域大小。Select the size of the Overlay Block area.

CPUx Overlay Mask Register i

OMASKi (i=0-31)
CPUx Overlay Mask Register i **($0FB18_H$+i*12)** **Application Reset Value: $0FFF FFE0_H$**



Field	Bits	Type	Description
RES	4:0, 31:28	r	**Reserved** Corresponding address bits are not used in the address comparison. Corresponding final address bits are taken from the original data address.
OMASK	16:5	rw	**Overlay Address Mask** This bitfield determines the overlay block size and the bits used for address comparison and translation. [...] "Zero" bits determine the corresponding address bits which are not used in the address comparison and thus determine the block size; corresponding final address bits are derived from the original data address. "One" bits determine the corresponding address bits which are used for the address comparison; corresponding final address bits are derived from RABRx register in case of address match. 000_H , 128 Kbyte block size 800_H , 64 Kbyte block size $C00_H$, 32 Kbyte block size FFE_H , 64 byte block size FFF_H , 32 byte block size
ONE	27:17	r	**Fixed "1" Values** Corresponding address bits are participating in the address comparison. Corresponding final address bits are taken from RABRx.

重映射掩码寄存器，主要是用来配置重定向区域大小的，共 12 个 bit，如图所示，Overlay 块大小只能是 2 的 n 次方的 32 个字节大小，范围是从 32B 到 128KB。

Overlay Mask Registers are mainly used to configure the size of an overlay block, a total of 12 bits, as shown in the above figure, the overlay block shall only be 2 n times the size of 32 bytes, the range is from 32B to 128KB.

6 OVERLAY 功能在 XCP 协议栈中的应用 APPLICATION OF OVERLAY IN XCP PROTOCOL STACK

6.1 XCP 协议概述 XCP OVERVIEW

XCP（Universal Measurement and Calibration Protocol）是 AUTOSAR 中一个重要的标准化协议模块，主要用于 ECU 的测量和标定。它采用主从架构，其中测试工具（如 CANape、INCA 等）作为主机，ECU 作为从机。XCP 支持多种通信方式，最常用的是基于 CAN 和以太网的传输。

XCP (Universal Measurement and Calibration Protocol) is an important standardized protocol module in AUTOSAR, primarily used for ECU measurement and calibration. It adopts a master-slave architecture, where testing tools (such as CANape, etc.) serve as masters and ECUs as slaves. XCP supports various communication methods, with CAN-based and Ethernet-based transmission being the most used.

XCP 模块的核心功能包括数据测量、在线标定、数据采集（DAQ）、内存读写以及程序下载等。它能够实时监控 ECU 内部变量，修改标定参数，并支持高速数据采集。在安全性方面，XCP 提供了多层次的保护机制，包括标定保护、DAQ 保护、编程保护和数据存取保护，确保 ECU 操作的安全性。

The core functions of the XCP module include data measurement, online calibration, data acquisition (DAQ), memory read/write, and program download. It can monitor ECU internal variables in real-time, modify calibration parameters, and support high-speed data acquisition. In terms of security, XCP provides multi-level protection mechanisms, including calibration protection, DAQ protection, programming protection, and data access protection, ensuring the security of ECU operations.

在实际应用中，XCP 模块广泛应用于汽车电子开发的多个阶段，特别是在 ECU 开发、测试和标定过程中。它不仅提供了标准化的接口，确保了不同工具间的兼容性，还支持灵活的配置选项，能够满足不同项目的需求。使用 XCP 时需要注意合理配置资源、考虑实时性要求、确保数据一致性，并注意带宽限制等因素。总的来说，XCP 模块是现代汽车电子开发中不可或缺的工具，能够显著提高开发效率和测试覆盖率。

In practical applications, the XCP module is widely used in multiple stages of automotive electronics development, especially in ECU development, testing, and calibration processes. It not only provides standardized interfaces ensuring compatibility between different tools but also supports flexible configuration options to meet the requirements of different projects. When using XCP, attention must be paid to reasonable resource configuration, real-time requirements, data consistency, and bandwidth limitations. Overall, the XCP module is an indispensable tool in

modern automotive electronics development, significantly improving development efficiency and test coverage.

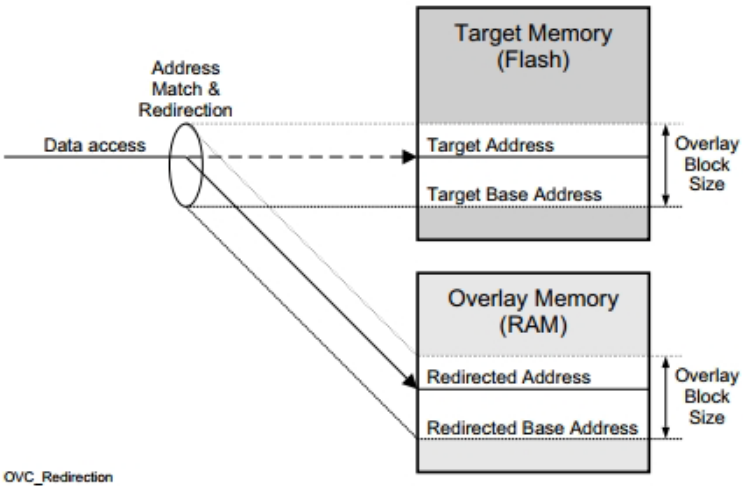
6.2 知从木牛的 XCP 协议栈产品与 OVERLAY 功能的配合 XCP MODULE OF ZC.MUNIU WITH OVERLAY FEATURE

知从木牛产品已实现符合 AUTOSAR R20-11 规范的 XCP 协议栈功能，并完成了在 TC3XX 平台上的移植和应用。标定时性能稳定，且易于集成和使用，能够有效支持汽车电子开发中的调试和标定需求，帮助控制器开发厂商提升效率，降低开发难度。

ZC.MuNiu Basic Software Platform has realized the functionality of XCP Module in accordance with AUTOSAR R20-11 specification, and has completed the transplantation and application on TC3XX platform. The measurement and calibration performance is stable and easy to integrate and use, which can effectively support the debugging and calibration needs in automotive electronics development, and help controller development manufacturers to improve efficiency and reduce development difficulties.

Data Access Overlay 最常见的用途之一便是应用在标定中。标定功能使用的木牛 XCP 协议栈其本质是为使用者提供了对 ECU 内部 memory 的读写机制。读访问保证了标定系统可以从 RAM 中读取观测量，即测量(measurement)；写访问保证了标定系统可以对 RAM 中的标定量进行数值修改，即标定(calibration)。

In practical applications, one of the most common uses of Data Access Overlay is for calibration functionality. The XCP protocol used in ZC.MuNiu XCP Module essentially provides users with a mechanism to read and write ECU internal memory. Read access ensures that the calibration system can read observables from RAM, known as measurements; write access ensures that the calibration system can modify the values of calibration parameters in RAM, known as calibration.



Flash 区标定数据的修改流程:

1. 上电时完成对各个核所需 Overlay 块区的初始化并使能需要数据标定的核的 Overlay 功能，并将划分好的 Flash 标定区域数据初始化拷贝到 Overlay 映射的 RAM 区;
2. 标定时，使得 ECU 对标定量的访问实际操作的是 RAM 的 Overlay Block 区域;
3. 标定结束后，通过上位机工具，如 CANape，生成标定好的 HEX 文件，并刷写进 FLASH 中完成整个对 Flash 区参数的标定过程。

The procesure of Flash calibration parameters:

1. At power-on, the initialization of the Overlay function for each core is needed, and the data located in Flash calibration area will be initialized and copied to the specific RAM area mapped by Overlay.
2. During calibration, the CPU's access to the calibration data operates on the Overlay Block area of RAM.
3. In the end, through an upper computer tool such as CANape, a calibrated HEX file will be generated and programmed into the FLASH to complete the entire calibration process of the Flash parameters.

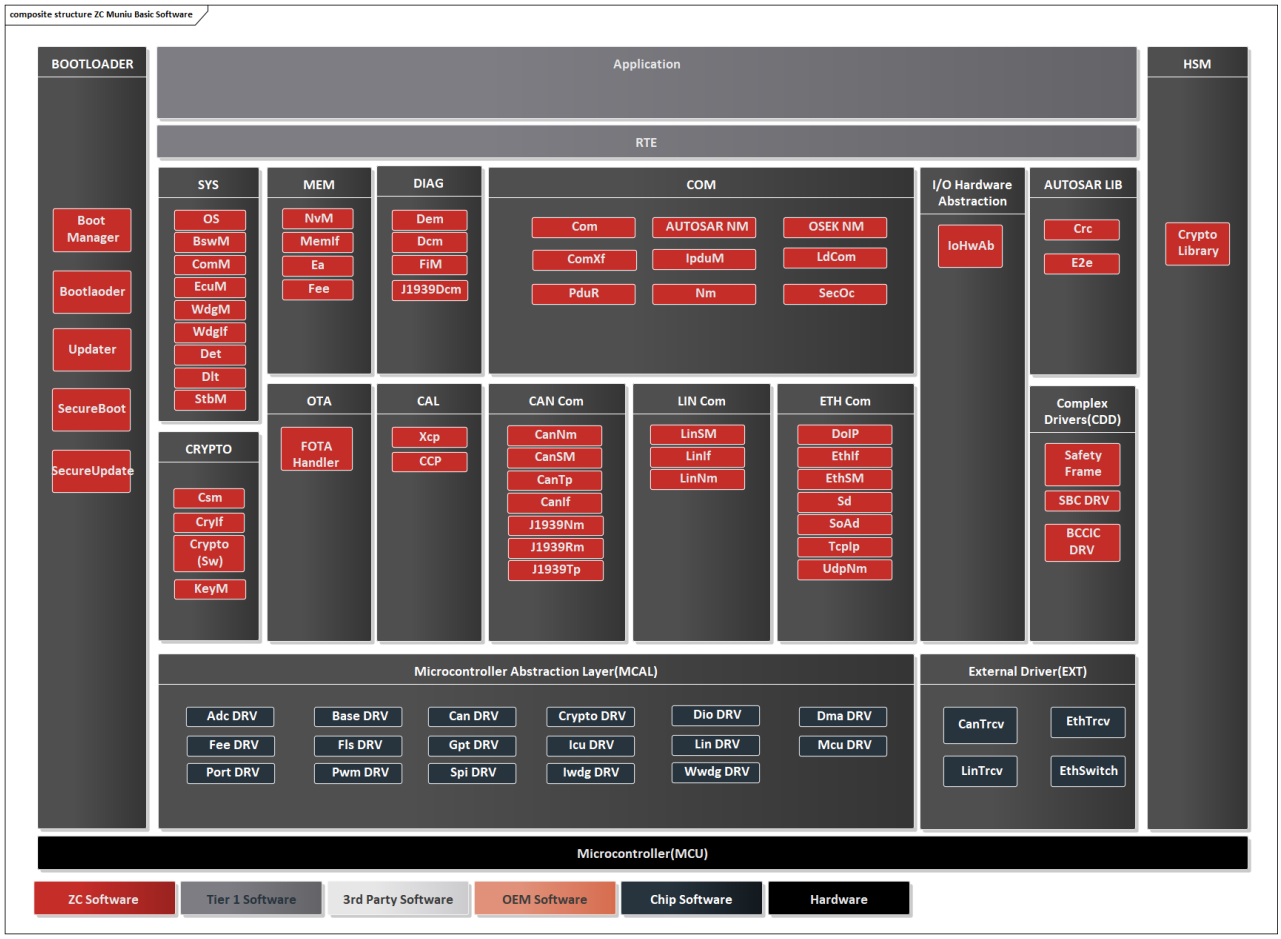
6.3 关于 ZC TC3XX 木牛基础软件平台的更多产品 MORE PRODUCTS AND FEATURE OF ZC.MUNIU BASIC SOFTWARE PLATFORM

- 符合 AUTOSAR R20-11 版本 Compliant with AUTOSAR R20-11 version
- ARTOP 架构上位机配置工具，最高适配 AUTOSAR R20-11 版本

  ARTOP architecture upper machine configuration tool, compatible up to AUTOSAR R20-11 version
- 多核操作系统 Muti-Core Operating System
- 通讯协议栈 Communication Protocol Stack（CAN\LIN）
- 诊断协议栈 Diagnostic Protocol Stack (UDS\J1939)
- 网络管理 Network Management (OSEK\AUTOSAR)
- 标定协议栈 Calibration Protocol Stack（XCP\CCP）
- 存储协议栈 Storage Protocol Stack
- 加密模块 Cryptography Module（CRYPTO）

- 复杂驱动定制开发 Custom Development of Complex Drivers
- 工程服务 Engineering Services

6.4 知从木牛基础软件产品软件架构 ZC.MUNIU BASIC SOFTWARE ARCHITECTURE



知从木牛基础软件平台架构

ZC.MUNIU BASIC SOFTWARE PLATFORM ARCHITECTURE

为了满足客户的不同项目需求，提高基础软件平台的扩展性，木牛基础软件平台实现了各个模块可配置性，并且实现了配置工具。客户可根据不同需求，在配置工具上完成各个模块的配置工作，可生成配置代码文件，将生成的配置文件集成到工程中即可。

To meet the diverse project requirements of customers and enhance the scalability of the basic software platform, the MuNiu basic software platform has implemented the configurability of each module and has also developed a configuration tool. Customers can complete the configuration of each module according to different needs on the configuration tool, generate configuration code files, and integrate the generated configuration files into the project.

木牛基础软件平台的配置工具是基于 Eclipse 平台，并基于 ARTOP 架构，实现 AUTOSAR 模型和 ARXML 的解析。除了 AUTOSAR 标准定义的模块之外，还支持 OEM 和 Tie1 厂商二次开发自己的模块。配置完成后，可生成各个模块的配置代码。

ZC.MuNiu basic software platform configuration tool is based on the Eclipse platform and is built on the ARTOP architecture, which implements the parsing of the AUTOSAR model and ARXML. In addition to the modules defined by the AUTOSAR standard, it also supports OEM and Tie1 manufacturers to develop their own modules for secondary development. After the configuration is completed, the configuration code for each module can be generated.

汽车在电动化、网联化、智能化的大趋势下，电子电器部件日益增多，电气结构越加复杂，整车开发周期不断缩短。平台化、智能化的基础软件起到至关重要。

In the major trends of electrification, connectivity, and intelligence, the number of automotive electronic and electrical components is increasing. The electrical structure is becoming more complex, and the development cycle of the vehicle is continuously shortening. Basic software plays an increasingly important role.

知从科技提供基础软件产品的同时，也提供符合 ASPICE Level 3 流程和功能安全 ASIL-D 要求的控制器基础软件功能实现的开发服务，SBC 芯片、BCCIC 芯片各种复杂驱动软件的定制开发。同时，集成知从科技的功能安全产品 SafetyFrame，可以满足功能安全要求。

ZC provides development services comply with ASPICE Level 3 processes and functional safety requirements of ASIL-D. ZC also provides customized complex driver software for SBC (Safety Control Board) chips and BCCIC (Battery Cell Control IC) chips. By integrating ZC's functional safety product SafetyFrame, the requirements for functional safety can be satisfied.

知从科技掌握 AUTOSAR 平台软件的开发和应用核心技术，提供本地现场支持，质量好，速度快，成本低。

ZC has the core technology of the AUTOSAR basic software and can provide on-site support with high quality, fast speed, and low cost.